

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a first multi-phased clock signal and (ii) two or more serial data signals; and

a second circuit configured to present said two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said first multi-phased clock signal comprises a bit clock signal.

3. (ORIGINAL) The apparatus according to claim 1, wherein said second clock signal comprises a reference clock signal.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said first circuit further comprises:

a third circuit configured to generate (i) one or more select signals and (ii) a selected clock signal in response to (i)

5 said first multi-phased clock signal and (ii) a phase select signal.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 4, wherein said first circuit further comprises:

5 a phase comparator circuit configured to generate said phase select signal in response to said one or more select signals and a first of said two or more serial data signals.

6. (ORIGINAL) The apparatus according to claim 4, wherein said third circuit comprises a phase generation and select circuit.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 5, wherein said first circuit includes a deserializer circuit configured to generate said parallel output data signal in response to said selected clock signal and a second of said two or more serial data signals.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said first circuit further comprises:

5 a multiplexer configured to generate (i) said first of said two or more serial data signals and (ii) said second of said

5 two or more serial data signals, in response to said two or more serial data signals.

9. (CURRENTLY AMENDED) A circuit comprising:

means for generating a parallel output data signal in response to (i) a selected phase a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals;
5 and

means for generating said two or more serial data signals and said multi-phased first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. (CURRENTLY AMENDED) A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased
5 first clock signal and (ii) two or more serial data signals; and

(B) generating said two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said multi-phased first clock signal is configured to control said pulse width.

11. (CURRENTLY AMENDED) The method according to claim 10, wherein said multi-phased first clock signal comprises a bit clock signal.

12. (ORIGINAL) The method according to claim 10, wherein said second clock signal comprises a reference clock signal.

13. (ORIGINAL) The method according to claim 10, wherein step (A) further comprises the sub-step of:

generating (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

14. (PREVIOUSLY PRESENTED) The method according to claim 13, wherein step (A) further comprises the sub-step of:

generating said phase select signal in response to said one or more select signals and a first of said two or more serial data signals.

15. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein step (A) further comprises the sub-step of:

generating said parallel output data signal in response to said selected clock signal and a second of said two or more serial data signals.

16. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

generating said first of said two or more serial data signals and said second of said two or more serial data signals, in response to said two or more serial data signals.

17-20 (CANCELED)

21. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said selected phase of said multi-phased first clock signal is selected in response to a phase selection circuit.

22. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein:

a phase generation circuit is configured to generate a said plurality of phases of said first clock signal.

23. (NEW) An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a first clock signal and (ii) two or more serial data signals;

a second circuit configured to present said two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal; and

a third circuit configured to generate (i) one or more
5 select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.